REMARKS

In the Office Action of November 17, 2004, claims 1-20 were presented for examination. Of these, claims 1 and 20 were rejected and claims 2-19 objected to for asserted informalities.

In light of the foregoing amendments and the remarks which follow, reconsideration is requested. Claims 1, 2, 9, 11, 15, 16, 19 and 20 are amended. No claims are added or cancelled.

Claim Objections

Page 2 of the Office Action states that claims 1-20 are objected to though the Office Action Summary states that claims 2-19 are objected to. Since there are specific objections to claims 1, 19 and 20, it is seen that the Office Action Summary is misleading as there is both a rejection and an objection against claim 1.

With respect to claims 1 and 19, the Examiner objects that the "thereby reducing..." language does not define any structure and accordingly cannot serve to distinguish. However, even if one accepts that statement (and Applicant neither accepts it nor refutes it), the fact that the words do not constitute a distinguishing limitation does not mean that the claim is informal or objectionable for including the language. It merely means the Examiner need not take those words into account in examining the claims for patentability over the references. (The same is true, for example, of intended use terminology in a preamble.) The language only serves to make the claim clearer. A "thereby" or "whereby" clause is perfectly appropriate to express an inherent result. The cited case law does not hold otherwise and does not support the objection. Applicant has not argued that the "thereby" clause in any way distinguishes over prior art. Accordingly, the objection is not well founded.

Nevertheless, to advance the prosecution of the application, claims 1 and 19 have been amended to remove the "thereby" clause at the end of each claim and to include in the first two lines of the claim a statement that the circuit is "configured to reduce the Early effect." Accordingly, claims 1 and 19 are now no longer even arguably objectionable.

For the record, Applicant has not amended claims 1 and 19 for any purpose relating to patentability, there being no rejection overcome by this amendment, and the Office Action

incorrectly considers the claims to contain informalities. Applicant does not intend the scope of claims 1 and 19 to be altered in any way by the amendments just discussed.

Claim 20 also received an objection. The Examiner stated that the "adapted to" language in the first line did not constitute a limitation (in the sense of affecting patentability). Again, the Examiner objects to language as not limiting where the language is clarifying and Applicant has not argued that it is limiting. There is no basis for the objection. The first two lines of claim 20 merely recite the nature of the method being claimed. Nevertheless, to advance the prosecution of the application, the word "adapted" has been replaced with the more concrete "configured", without any intention of altering the scope of the claim. This amendment to claim 20 is not required for purposes of patentability, only to cure an apparent informality.

It should now be seen that none of claims 1-20 was or is objectionable. Accordingly, withdrawal of the objections is requested.

Claim Rejections - 35 USC §102

Claims 1 and 20 have initially been rejected under 35 USC §102(b) as anticipated by Joseph, U.S. Patent 4,399,399. The rejection is unfounded and reconsideration is requested.

For a claim to be anticipated under 35 USC 102(b), a single reference must show each and every limitation of the claimed subject matter. Here, the claimed subject matter is a bandgap voltage reference circuit (claim 1) and a corresponding method of providing a bandgap reference voltage circuit (claim 20) which reduces the Early effect of the transistors in the circuit. The bandgap voltage reference circuit provides at the output of an amplifier a buffered *voltage* reference. Joseph, however, does not disclose a voltage reference. It discloses a *current* reference. Manifestly, the provision of a current reference is not the provision of a voltage reference. Consequently, Joseph does not anticipate either claim 1 or claim 20 and is not even opposite or analogous prior art.

The Office Action should have mapped each limitation of claims 1 and 20 against Joseph. Instead, it only listed parts and ignored their interconnections and functions.

As a consequence, the Examiner failed to spot that difference. To turn Joseph from a current reference into a voltage reference would require a major redesign that still would not

achieve the claimed invention. If one were to reconfigure the current reference of Joseph to a voltage reference, one could replace the LOAD 34 with a resistor/transistor combination. However, (a) this is hindsight and (b) the result would be an unbuffered voltage reference, not the buffered voltage reference that is explicitly claimed.

Further, the configuration in Joseph does not provide for a reduction in the Early effect, which is explicitly provided by the claimed invention. The Early effect, of course, is the reduction of the width of the base region in a bipolar transistor due to the widening of the base-collector junction area with increasing base-collector voltage. The Early effect may be observed on the output characteristics (collector current versus base-collector voltage) as a slight increase of the collector current out of the saturation region. In Joseph, the base-collector voltage on transistors 18 and 20 are at the same level, but transistors 12, 14 and 32 are exposed to Early effect, depending on the supply voltage Vcc . In the claimed invention, transistors 12, 13 and 14 are not present and, therefore, cannot provide an Early effect contribution to the output of the circuit.

Manifestly, therefore, claims 1 and 20 are patentable over Joseph. Reconsideration and withdrawal of the rejection are accordingly requested.

Claim Rejections - 35 USC §103

Claims 1 and 20 also have been rejected under 35 USC 103(a) as obvious over the admitted prior art (APA) of Figure 1 in view of Dosho et al, U.S. Patent 5,751,142. Applicant has reviewed the rejection, disagrees and requests reconsideration.

In supporting the rejection, the Office Action states that "APA figure 1 discloses the claims subject matter regarding claims 1 and 20 except for a diode connected transistor." It then offers Dosho as teaching connecting diodes to the inputs of amplifiers and the formation of diodes by connecting the base of a transistor to its source or emitter. Then the Examiner reasons that it would have been obvious to modify APA Fig. 1 to include a diode connected transistor coupled to one of the inputs of an opamp as taught by Dosho et al "in order to block reverse currents coming from ground." On closer inspection, the rejection reveals an arbitrary extraction

of features from one circuit and their superimposition onto another circuit, in order to address a nonexistent problem that is not even solved by the present invention.

There is no motivation to modify either reference contained therein or anywhere else in the art. Moreover, even if they are combined, their combination does not yield the claimed invention. APA figure 1 is, indeed, a bandgap reference source providing a voltage reference output. It does include an amplifier and two transistors. The bases of the two transistors are commonly coupled. However, it differs from the claimed invention in that it does not show one of the first and second transistors being provided in a diode-connected configuration while the base-collector voltage of the other transistor is maintained at zero by the amplifier coupled in a feedback loop to the collector of each of the transistors.

By controlling the base-collector voltage of each transistor and, in fact, by making that voltage zero, the present invention addresses the Early effect. That is at least in part the purpose of the diode connection of the first transistor, but it also requires the control of the second transistor.

The Office Action suggests that the combination of APA Figure 1 with a diode-connected transistor as provided in Dosho would result in the present invention. That is simply incorrect.

Dosho does provide for diodes, but that is about as far as it goes. There is no teaching of the Early effect, its importance or how to minimize it. The circuit is based on diodes. The formation of a diode by coupling the base of a transistor to its collector is nothing more than what has been known for decades by practically any undergraduate electrical engineering student. Diodes are known for blocking currents; and if this had been a problem with the Brokaw cell of APA Figure 1, then possibly someone might have been motivated to put in a diode to block current leaking from ground. However, this is <u>not</u> a problem with the Brokaw cell and any suggestion otherwise by the Examiner is a mere hindsight attempt to justify his unfounded assertion that a person of ordinary skill in the art would have turned to Dosho and modified it in light of the disclosure of APA Figure 1.

However, in the Brokaw cell of APA Figure 1, the current always goes from the supply voltage or reference to ground, not the other way around! Therefore, there is no requirement to provide a diode-connected transistor to block a current leaking from the ground. As there is no

motivation to connect a diode-connected transistor, why would one replace transistor Q2 of the Brokaw cell with a diode-connected transistor? There would be no motivation. The Examiner has suggested that there is motivation to prevent current leakage from ground; but, as stated above, that is not really a problem and it therefore cannot provide motivation.

The diode-connected transistor of the present invention is there to control the base-collector voltage of the transistor, not to prevent current leakage. It is to minimize the Early effect.

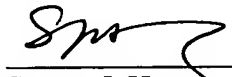
The problem and its solution, as provided and claimed herein, is only realised once one has reviewed the instant disclosure. That is, by applying a hindsight analysis. Hindsight is prohibited by all of the case law explaining §103.

There is no teaching of the advantage of the specific configuration of both transistors as provided for in the claimed invention, so as to control their base-collector voltages, from either APA Figure 1 or Dosho, alone or in combination. Consequently, there is no support for a suggestion that one skilled in the art would have combined the two references to arrive at the claimed invention. The rejection should therefore be reconsidered and withdrawn.

If for any reason this communication is not seen to put the application in condition for issuance of a Notice of Allowance, the Examiner is requested to contact the undersigned by telephone, collect, to discuss how prosecution may be advanced toward allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,



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